Single-Event Effect Performance of a Conductive-Bridge Memory EEPROM

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***Abstract*—We investigated the heavy ion single-event effect (SEE) susceptibility of the industry's first stand-alone memory based on conductive-bridge memory (CBRAM) technology. The device is available as an electrically erasable programmable read-only memory. We found that single-event functional interrupt (SEFI) is the dominant SEE type for each operational mode (standby, dynamic read, and dynamic write/read). SEFIs occurred even while the device is statically biased in standby mode. Worst case SEFIs resulted in errors that filled the entire memory space. Power cycle did not always clear the errors. Thus the corrupted cells had to be reprogrammed in some cases. The device is also vulnerable to bit upsets during dynamic write/read tests, although the frequency of the upsets are relatively low. The linear energy transfer threshold for cell upset is between 10 and 20 MeV·cm^2/mg, with an upper limit cross section of 1.6 × 10^{-11} cm^2/bit (95% confidence level) at 10 MeV·cm^2/mg. In standby mode, the CBRAM array appears invulnerable to bit upsets.**

***Index Terms*—Single-event effect, non-volatile memory, heavy ion testing, radiation effects in ICs.**

I. Introduction

Conductive-bridge random access memory (CBRAM) is a programmable metallization cell (PMC) memory in the family of resistive memories [1]−[4]. The scaling limitations of flash spurred the introduction of alternative non-volatile memory technologies. The CBRAM has shown advantages in performance and scalability relative to other alternative non-volatile memory technologies [2]. Additionally, the resistive elements can be fabricated back-end-of-line (BEOL) on CMOS processes [1]. Therefore, it can be more easily integrated into existing CMOS wafer fabrication lines. The rapid development in resistive memories has expedited the release of commercial-ready products. The CBRAM from Adesto is an electrically erasable programmable read-only memory (EEPROM) [1], [4]−[5].

EEPROMs have been and continue to be widely used in space flight systems for data and code storage [6]−[10]. However, options for space-grade devices are limited. EEPROMs based on charge-trap technology (i.e. Silicon-Oxide-Nitride-Oxide-Silicon (SONOS)) are more radiation tolerant than floating-gate technologies. However, they are still vulnerable to total ionizing dose (TID) and single-event effects (SEE). In particular, currently available radiation tolerant EEPROMs can still be susceptible to destructive single-event dielectric rupture (SEDR) in the charge pump transistors [11], [12]. Additional process and/or design changes are needed to enhance radiation tolerance for both charge-trap and floating-gate devices.

The CBRAM offers a promising alternative to traditional charge-trap or floating-gate technologies for space applications, due to its intrinsic radiation tolerance. Previous studies found that the CBRAM from Adesto Technologies is free of errors following statically biased irradiation up to 450 krad(GeS_2) of gamma rays, and up to 3 Mrad(CaF_2) of 10 keV x-rays [13], [14]. The device is also hardened against displacement damage up to 10^{14} n/cm^2 of 1 MeV equivalent neutrons [14]. Other studies found that single-event upset (SEU) at the cell level can occur, due to upset of the access transistor [16]−[17]. However, those studies were carried out on test chips or devices with bias configurations not intended for practical applications. We have previously investigated the SEE performance of a microcontroller with embedded reduction-oxidation memory [15]. We found that single-event functional interrupt (SEFI) dominated the SEE response, and bit upsets, while possible, are extremely rare under normal operating conditions [15]. There is yet to be a comprehensive SEE evaluation of a stand-alone resistive memory product. Here, we investigate the SEE susceptibility of the Adesto CBRAM EEPROM, the first stand-alone memory based on CBRAM technology.

II. Experimental

A. Device technology

The RM24C series EEPROM from Adesto Technologies is the industry's first stand-alone memory built with CBRAM technology [1], [4]−[5]. The EEPROM is available in 32, 64 or 128 Kb in a 8-lead Small Outline Integrated Circuit package. The endurance specification limit is guaranteed for 25,000 write cycles. The device is accessed through a 2-wire

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I^2C compatible interface consisting of a Serial Data and Serial Clock. The maximum clock frequency is 1 MHz. Figure 1 shows a microphotograph of the die from a third generation device. Figure 2 shows a schematic diagram of the one-transistor-one-resistor (1T1R) architecture of a CBRAM cell. To program a cell, the Word Line (WL) and Select Line (SL) (also the CBRAM anode) is High. The Bit Line (BL) pulses High to Low, which forward biases the CBRAM. To erase a cell, the WL is high, and the SL is low. The BL pulses Low to High, which reverse biases the CBRAM.

The CBRAM is fabricated BEOL on a 130 nm commercial Complimentary-Metal-Oxide-Semiconductor (CMOS) process. Figure 3 shows a transmission electron microscopy (TEM) image of the device cross section, with the CBRAM stack magnified in the bottom image. The CBRAM stack is located near the top of the structure. The CBRAM connects through metal vias to the CMOS elements at the bottom. The composition of the CBRAM have evolved for each device generation.

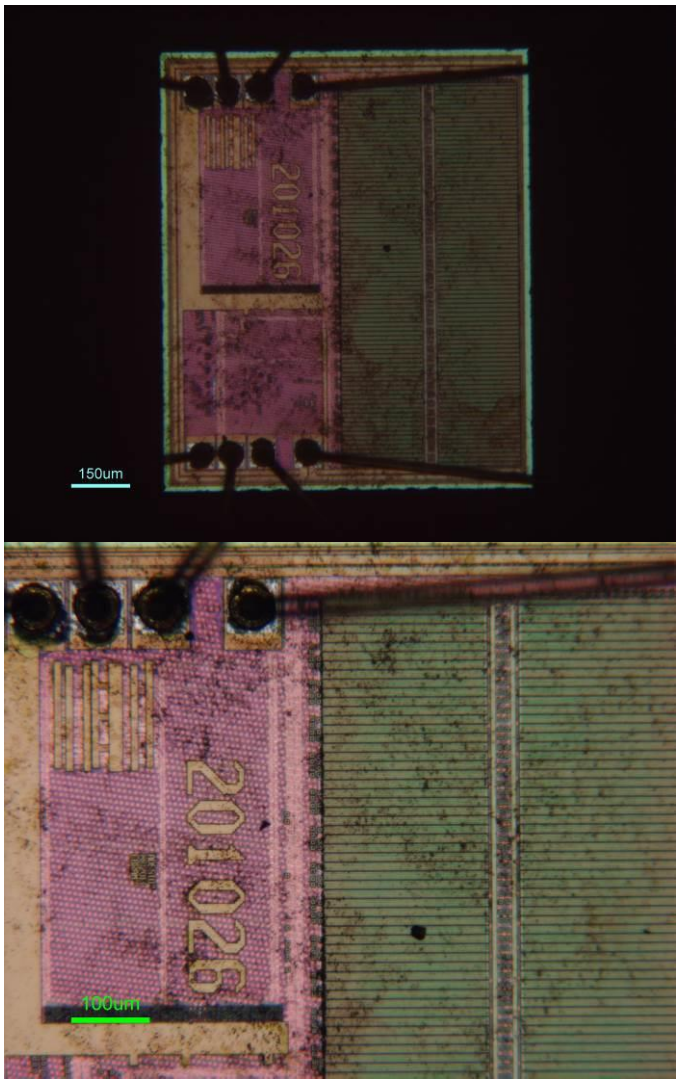

Figure 1. Schematic block diagram of internal functional elements.

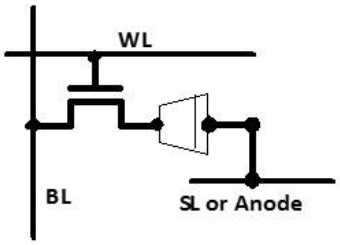

Figure 2. 1T1R implementation of the CBRAM. Program: WL and SL are biased High. BL pulses High to Low. Erase: WL is High. SL is Low. BL pulses Low to High.

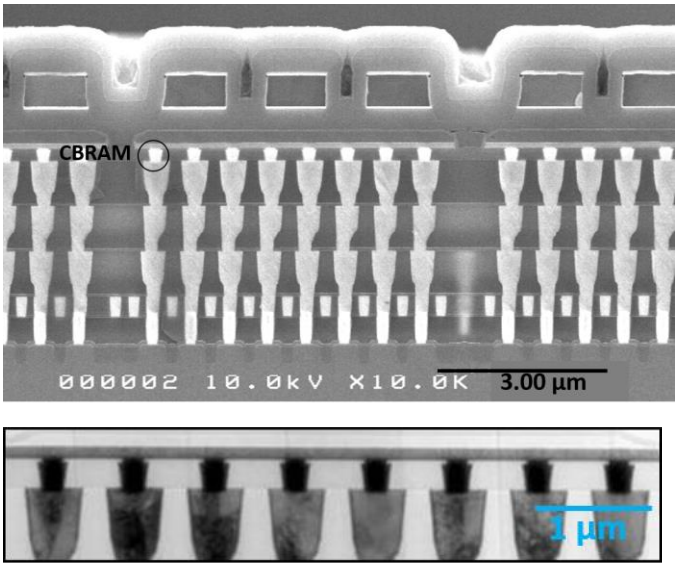

Figure 3. TEM image of the CBRAM cross section. Bottom image magnifies the CBRAM stack. (*courtesy of Adesto*)

B. Test methodology

We interface with the CBRAM using an ARM Cortex-M4-based 32-bit microcontroller with 64kB RAM and 256kB flash memory. A PC sends/receives commands to/from the microcontroller. Figure 4 shows a photograph of the test board mounted inside the irradiation chamber. The device-under-test (DUT) is soldered onto a two-sided copper-plated socket. We programmed the memory with a repeating pattern: 00, FF, AA, 55, or counter. The test modes include: static on (standby), continuous read, and continuous write/read. The read mode included byte (random) read and sequential read. The write mode included byte write and page write. We actively monitored the supply current during irradiation. The test procedures are as follows:

1. Configure the CBRAM with the desired test mode
2. Irradiate the DUT to a desired fluence (typically 2×10^6 cm^{-2} /run) or until functional error
    a. In case of a functional interrupt, attempt to recover device operations with a second read
    b. If errors remain, then power cycle DUT
    c. If errors remain, rewrite to DUT
3. If the DUT remains functional, repeat 1 and 2 for the next test condition

We irradiated four parts in vacuum at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility with a cocktail of 16 MeV/amu heavy ions. Table I shows the heavy ion beam information, including the ion species, energy, linear energy transfer (LET), and range. We also carried out pulsed-laser testing at the Naval Research Laboratory with a 590 nm single photon dye laser. The test samples were acid-etched to expose the die surface.

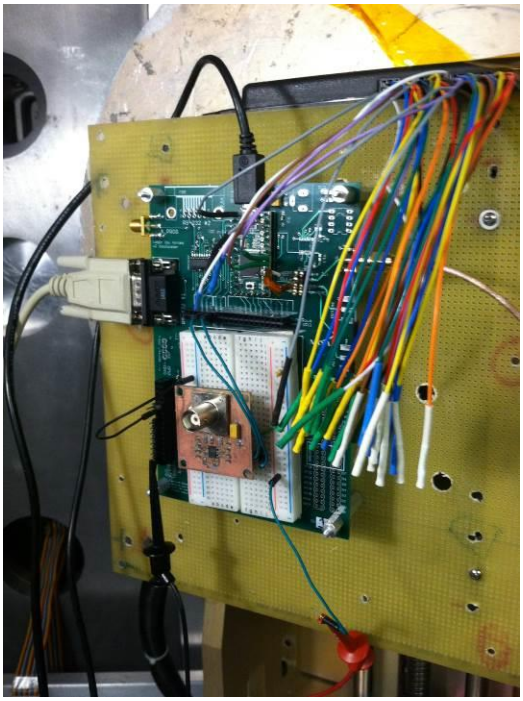

Figure 4. Photograph of the test setup inside the LBNL irradiation chamber.

Table I.
Heavy ion species, energy, LET, and range.

Ion	Total Energy (MeV)	LET (MeV·cm^2/mg)	Range in Si (μm)
Ne	253	3.1	225
Ar	642	7.3	256
Kr	1225	25.0	165
Xe	1955	49.3	148

III. Results and Discussion

A. Single-bit upset

We observed SEUs that are characteristic of ion-induced upsets in the memory array. Previous studies showed that although the resistive memory cell is extremely tolerant against ionizing irradiation, radiation-induced cell upset is possible under the appropriate electrical and ion beam conditions [16]−[17]. Cell upset can be caused by SEU of the access transistor. However, the operation principals of the CBRAM dictate that the device is much more vulnerable during write or erase than during read or standby. In contrast to previous tests performed on test structures under constant bias conditions, here we examine a complete product under dynamic bias conditions.

We filtered the errors to distinguish the single-bit upsets (SBU) from errors caused by single-event transients (SET) in the peripheral circuit. For example, we did not include SEUs which can be cleared by a second read during read-only tests. These errors are likely due to data corruption in the buffer. There were only four SEUs of this type. We also did not include the SEUs that cleared after a power cycle. These errors originated from upsets in peripheral control circuits, which lead to operational errors. Finally, we did not include errors with multiple errant bits.

Figure 5 shows the SBU cross section as a function of LET for each ion species. The error bars herein represent the Poisson errors at 95% confidence level. The relatively high error standard deviations are due to low count. The SBU cross section generally increases with effective LET. The LET threshold is approximately between 10 and 20 MeV·cm^2/mg. The upper bound cross section at 95% confidence level is 1.6×10^{-11} cm^2/bit at LET of 10 MeV·cm^2/mg. Additionally, we did not observe any discernable angular dependence, within the Poisson error deviations. As can be seen, the cross sections are similar for Kr at 60° and Xe at normal incidence for a LET of 60 MeV·cm^2/mg.

Moreover, we only observed the SBUs during write/read tests, not during static or read-only test modes, a characteristic that is consistent with previous studies of the CBRAM and other resistive memory technologies [16]−[17]. Consequently, the error rate that is directly derived from the cross section in Figure 5 will be further scaled down according to the duty cycle of the application.

The SBUs consisted of both 1 to 0 and 0 to 1 type errors, where 1 and 0 represents the high and low resistive states, respectively. The bit error characteristics differ from previous observation that 0 to 1 errors (high resistive state to low resistive state) would be dominant [16]. It is important to highlight that there are differences in the operation mode of the product here than the test structures from previous tests. Here a cell's most vulnerable state is during erase rather than program, provided that a bit flip is caused by a SEU from the access transistor. The vulnerable off-state transistors are located in the same row (sharing the same bit line) as the target cell to be erased. A transient current from the drain will momentarily turn on the transistor and reverse bias the CBRAM stack. Consequently, a SEU will likely change a cell from a low resistive state (1) to a high resistive state (0). Errors of the opposite polarity will be less likely.

With that said, we observed SEUs of both polarities. We note that the total number of write cycles are kept below the 25,000 endurance specification limit. So the cell corruptions are independent of reliability failures. Some of the SEUs may represent undetected buffer upsets, since the errant bytes are immediately rewritten on the next write cycle. More importantly, a larger sample size is needed to reveal a more representative upset characteristic. The low probability of these events reflect the CBRAM's robustness against ion-induced cell upsets.

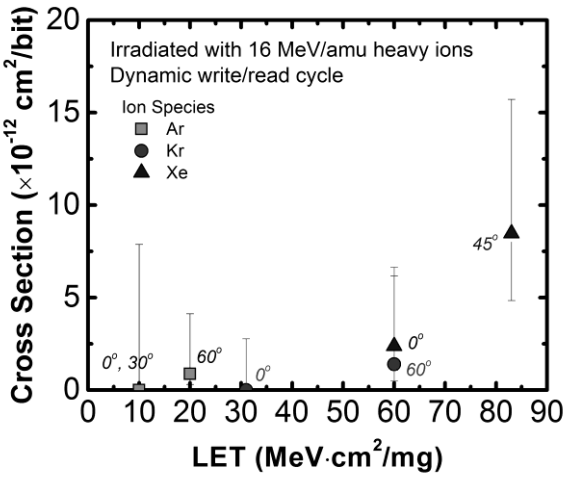

Figure 5. SBU cross section per bit vs. effective LET for each ion specie. SBUs were only observed while the device is continuously exercised in write/read cycles. Error bars represent the limits at 95% confidence level.

B. Single-event functional interrupt

We observed SEFIs while operating the device in static (standby) and dynamic test mode. Figure 6 shows the SEFI cross section as a function of effective LET for both test modes. The continuous read and write/read tests produced similar cross sections. So the data are averaged for the dynamic test mode. The data from static mode represent the upper limit cross sections, based on each run's predetermined fluence levels. The SEFI LET threshold is below 10 MeV·cm^2/mg.

Whereas single-bit errors may be invisible to the system, since they can be corrected via error correction algorithms, SEFIs can often result in system-level impacts. Perhaps the two most relevant questions for system reliability and mission assurance are: 1) will data be lost? and 2) how do we recover? Table II categorizes the SEFIs with respect to the test mode, recovery method, data loss, and error signature.

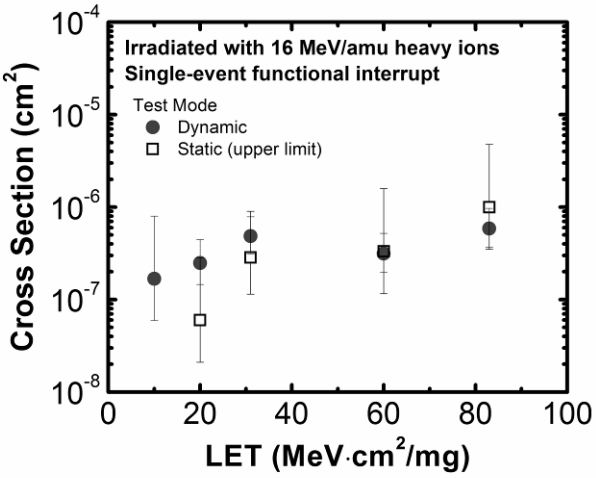

Figure 6. SEFI cross section vs. effective LET for parts irradiated while continuously exercised or statically biased. The cross sections for statically biased case represent upper fluence limits.

Table II
SEFI characteristics.

Test Mode	Recovery method	Data Loss?	Characteristics
Dynamic	Cleared on next read	No	1) address counter offset by 1 byte throughout read in one case 2) random and FF errors in other cases
Static and Dynamic	Power cycle	No	1) mass errors that read all 00 or FF 2) a stuck address error 3) a stuck bit error.
Static and Dynamic	Rewrite	Yes	1) mass errors that read all 00, FF, or random values. 2) errors changed values following power cycle to FF in one case, and to random values in another case.

The most common type of SEFI resulted in the entire memory reading FFs. The next most common type of SEFI resulted in mass 00 errors. These SEFIs could be recovered with a power cycle in most cases. However, for some events, a portion of the errors remained even after a power cycle (loss of data). Figure 7 shows the error bit map from such an event following static irradiation. The x-axis shows the address, scaled by a factor of 8. The y-axis represents data bytes in 8 bit columns. Each marked data point represents a bit error. Here the cells were originally programmed to a repeating AA pattern prior to irradiation. After the irradiation, all of the memory space read FF. Hence, each the bits in alternate row originally programmed to 0 appear as errant bits, as shown in Figure 7 (top). A power cycle cleared most of the errors, except for two pages and two SEUs, as shown in Figure 7 (bottom). These errors may signify data corruption. In other cases, the error manifest in one page or several consecutive pages. The fact that the errors are not distributed uniformly in the memory space indicate that they are caused by peripheral circuit errors rather than ion-induced cell upsets.

Furthermore, we observed the supply current spikes of $2-3$ mA during irradiation likely indicative of signal contention [18].

A few of the SEFIs that occurred in write mode had some unique characteristics apart from those observed during read only mode, including 1) an inability to write, and 2) functional hang-up due to I^{2}C acknowledgement fails. These SEFIs required power cycle for recovery.

The SEFIs can significantly impact system availability. In a typical application the EEPROM will remain in standby mode throughout the majority of a space mission. The memory will be read from occasionally, and rarely written to on-orbit. Thus, static mode SEFIs are particularly concerning. It is also important to evaluate the SEE characteristics in the dynamic test mode despite the low duty cycles, due to the increased susceptibility to SEFIs and destructive SEEs.

The recovery method often determines the severity of a SEFI. Data buffer errors can be dealt with by performing a second read, while control circuit errors may require a power cycle. An unplanned power cycle can impact the space system at a

board, box, or instrument level. It could leave a science instrument temporarily inoperable, missing valuable data recording. Additionally, the recovery process for the errors that require rewrite will be time consuming. In Figure 8 we examine the frequency of each type of SEFI according to its recovery method. We did not find significant differences in the upset cross sections for the different categories of SEFIs, given the Poisson error deviation.

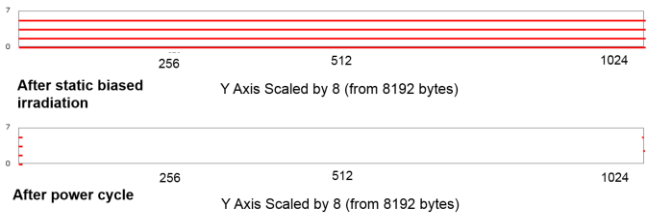

Figure 7. (top) Error bit map following static exposure. (bottom) Error bit map after a power cycle. X-axis shows the address, scaled by a factor of 8. Y-axis represents data bytes in 8 bit columns. Each marked data point represents a bit error. Here the cells were originally programmed to a repeating AA pattern prior to irradiation. The SEFI caused the entire memory to read FF. Hence the errors show in each alternate row. A power cycle cleared most of the errors, except for two pages (34 addresses) and two other address errors.

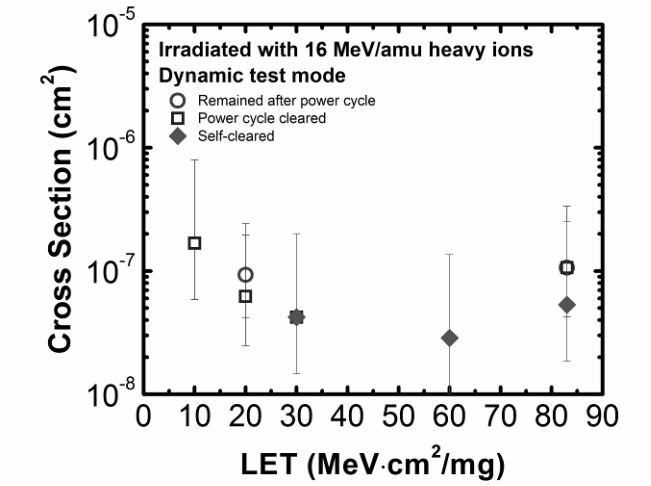

Figure 8. SEFI cross section vs. effective LET. SEFIs categorized with respect to recovery method.

C. Pulsed-laser

In addition to heavy ion testing, we carried out pulsed-laser testing at the Naval Research Laboratory. We used a 20× and a 100× lens with spot size of 1.7 µm and 0.9 µm, respectively. Much of the peripheral circuits were covered with metallization as evident in Figure 1. So the pulsed-laser cannot completely penetrate into some sensitive regions. This prevented correlation of laser energy with the corresponding heavy ion LET. However, the pulsed-laser deposited enough energy to trigger SEE in several spots on the die. We were able to observe SEFIs with characteristics similar to those seen in the heavy ion test.

Notably, we did not observe errors from the memory array. This is not surprising given the rarity of SEUs during heavy ion testing. All of the SEFIs originated from strikes in the peripheral circuits, including the bandgap reference, voltage regulator, static random access memory, and logic circuits.

In addition to the CBRAM cells, the memory array consisted of input/output buffers, sense amplifier and write circuits. In contrast to a previous investigation on an embedded resistive memory device, strikes on the sense amplifier circuits and write circuits did not lead to upsets [15]. The sense amplifier circuit was one of the most sensitive locations in [15]. The differences in program/erase/read pulse frequencies can lead to a reduced vulnerability window for the CBRAM. Another possible explanation for the relative insensitivity may be the partial obstruction of the laser beam by the top metallization. Nonetheless, the pulsed-laser test showed that the CBRAM array is robust against ionizing radiation-induced upsets. The test also aided in identifying some of the peripheral circuits that are sensitive to SEFIs.

IV. Conclusion

We have evaluated the heavy ion SEE performance of a novel stand-alone CBRAM EEPROM. While SEFI was the dominant error mode, we also observed bit upsets from the CBRAM array. The upsets occurred only during write/read cycles, a characteristic that is consistent with previous studies on resistive memories [15]−[17]. We did not observe bit-upset when the device is unpowered, in standby mode, or during a read operation. The radiation tolerance contrasts with floating-gate or charge-trap flash and EEPROMs. This characteristic offers an unique advantage for the potential utilization of the CBRAM in space applications.

The SEFI susceptibility and signatures are similar to other memory technologies. The fact that the CBRAM is fabricated BEOL on a standard CMOS process allows the industry to develop the technology into a space grade product. The manufacturer or other appropriate military/space chip manufacturers can potentially transfer the CBRAM technology onto a radiation-hardened platform without a complete redesign of the fabrication process. This distinction offers another advantage for the CBRAM's potential utilization for space missions.

Nonetheless, there are areas that need further exploration and continued evaluation. For example, the effects of cumulative radiation (total ionizing dose and displacement damage) on endurance and retention deserves investigation. As we have seen for NAND flash, total ionizing dose can reduce the data retention and increase error rate by several factors [19]. Additionally, the memory architecture for a high density CBRAM device will likely differ from the device studied here. The dimensions of the CBRAM stack will shrink with continued scaling, accompanied by reduction in the cell-to-cell noise margin. Both elements can impact radiation sensitivity.

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